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A Pipelined Implementation of Fixed Point Reversible Modular Non-Restoring Square Rooter on FPGA

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ABSTRACT: In present scenario size of the Computational devices and speed of operation has been a very alarming prospect, Reversible logic technology provides solution for this problem. Arithmetic square root is perhaps the most vital and complex computation in applications such as numerical analysis and signal processing. Generally square root structures are irregular which makes their implementation in hardware a difficult task. In this project a pipelined modular non restoring square rooter using parity preserving reversible gates has been proposed with the help of which results for any number of word length can be realized. The proposed architecture's functionality has been verified using Modelsim 5.7g for 8,16,32and 64 bit respectively. Parameter analysis for different word lengths such as quantum cost, number of gates have been calculated and hardware utilization were analyzed using Quartus-II 9.0 with respect to Stratix-II device along with EP2S15F484C5 family.It was found that as the word length increases the efficiency improvement for, the Pipelined Modular Non-Restoring Square rooter (MRNR) among 8, 16, 32and 64 bits were 10.7%,27.2%,38.25% and 46.21% respectively. Moreover 64-bit pipelined MRNR using KMD gate4 utilizes lesser hardware when compared to F2PG gate and Islam gate by 18.80% and 18.87% respectively.

KEYWORDS: Reversible logic, Parity preserving, Square rooter,pipelined implementation.

I. INTRODUCTION

The square root is a fundamental mathematical operation that has a wide variety of applications. Computer graphics, "GPS" global positioning systems, digital signal processing (DSP) calculations and math operations all require square roots.Low Power is the most significant innovation in the field of VLSI in the modern world of advancements in a variety of fields.Because the number of output and input ports in irreversible logics is not consistent, there will be information bit loss According to Launder's Theorem [1], a single bit of information consumes kTln2 Joules of energy computing must be reversible in order to prevent energy and data loss [2]. The authors of [3] devised a reversible nonlinear feedback shift with minimal power consumption.More hardware resources are required for the restoring technique, whereas less hardware is required for the non-restoring approach.As a result, the non-restoring algorithm [5] is preferable. Using irreversible logic, various reversible logic circuits are utilized in the calculation of digit-by-digit square root.Array-based arithmetic computations can potentially result in suboptimal performance [6].The number of iterations is directly related to the precision of these algorithms and only calculates the square root of digits at a time.An array of simple computational modules is usually used to implement these methods in hardware. The Step is executed once for every array row. This procedure executes once per array row. Designing an integrated circuit with a massive number of transistors has always been timeconsuming and costly. The design process is greatly simplified if these circuits are made up of a number of simple and recurring components.Pipelining is the collection of processor instructions via a pipeline. It permits storing and executing instructions sequentially. The pipelining technique is used to improve the time complexity of the gates in Modular Non-Restoring Method.

1.1 Reversible Locig and Parity Preserving

The fundamental premise of reversible logic is one-to-one mapping.Equal inputs and outputs are present in a reversible logic circuit.Reversible logic is utilized in upcoming technologies such as Quantum Computing, Optical Computing,

Nano Technology,and Digital Signal Processing to prevent information loss during operations [1]. The parity-preserving property is most commonly utilized in digital systems, and it allows a circuit to detect both permanent and parity signals. Parity-preserving gates, where the input parity is identical to the output parity, can be used to provide this fault tolerant/detection method[2].

The paper is structured as follows: Section II discusses a several reversible logic primitive, as well as certain performance metrics.

The reversible gates which are implemented in the proposed modular non-restoring method are described in Section III. Section IV gives the detail information about the proposed method architecture and their reversible components. In Section V, the outcomes of the simulations are reviewed, while Section VI contains a list of references.

1.2 Quantum cost

The quantum cost of a reversible gate is the number of reversible or quantum gates required for the architecture and ranges from 1x1 to 2x2. Quantumunit cost exists in all reversible 1x1 and 2x2gates [6].

1.3 Garbage outputs

The number of outputs that are not used to expedite the calculation is known as garbage output. It's mostly utilized to keep reversibility.

1.4 Constant input

Constant input is the usage of a constant logical 0 or 1 as the input to a reversible circuit. In a reversible circuit, the garbage outputs and constant inputs are completely reliant on the gates. [3].

II. REVERSIBLE GATES

The reversible gates used in this paper are

1. KMD gate4
2. F2PG
3. Islam gate

KMD gate4

The input vector is I (A, B, C, D, E) and the output vector is O (P, Q, R, S, T). The verification is based on the constant output (A). It is 5*5 paritypreservingreversiblegate. The KMD gate4 is depicted inthe Fig.1.

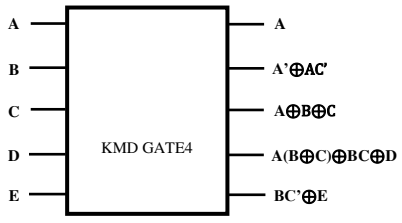

Fig. 1 KMD Gate4

The outputs of the KMD gate4 are P=A, Q=A'B+AC' and R=A^B^C, S=A(B^C)^BC^D, T=BC ' ^E. Quantum cost of a KMD gate4 is 12[10].

Parity preserving Full Adder:

The fig.2 depicts the block diagram of KMD gate4 functioning like a full adder. The resultant sum and carry are computed using A, B, and C as inputs. The other two inputs are provided with constant input of '0'.

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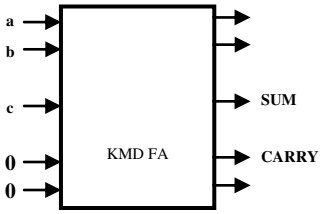

Fig. 2 KMD Gate4 Full adder

The full adder has fiveconstant inputs and five garbage outputs and thecorresponding Boolean expressions are listed below,

$$\text{Sum} = A \oplus B \oplus C$$
$$\text{Carry} = A(B \oplus C) \oplus BC \oplus D$$

III. MODULAR NON-RESTORING SQUARE ROOTER

The procedure to calculate the square root of a number could be achieved using the non-restoring square root algorithm which involves five various steps.

Input - 2n-bit operand.
Output - n-bit quotient Q
n-bit remainder S
Step 1: $S_0=0.y_1y_{2;}G_0=0.01$; j=1;
Step 2: $S_1=S_0-G_0$;
Step 3: If (S_j<0), then ($q_j \leftarrow 0; S_j \leftarrow S_j.y_{2j+1}y_{2j+2;}$
$G_j \leftarrow 0.0...0q_1q_2...q_j11$; $S_{j+1} \leftarrow S_j+G_j$;) Else ($q_j \leftarrow 1$; Sj
$\leftarrow S_{j.}\ y_{2j+1}y_{2j+2;}G_j \leftarrow 0.0...0q_1q_2...q_j01$; $S_{j+1} \leftarrow S_j-G_j$;)
Step 4:j← j+1;
Step 5: If (j≤ n) then (go to step 3)
Else ($Q=0.q_1q_2q_3...q_n$);
End;
Initialization of the algorithm takes place between Steps 1 and 2. After S1 is formed, steps 3 through 5 of the proposed method are reiterated. At each iteration, two bits of the operand are appended to the partial remainder fr. The square root bits are in contrast. The previous step to form Si was shifted and enlarged with two constant digits of 01 or 11 to produce the variable Gi. qi is decided according to the value of Si. Either the next partial remainder Gi is incorporated to Si to produce the result Gi, or Si+1 is produced.

3.1 Internal architecture of RCAS block

The main blocks of modular non- restoring square rooter are RMAAS-1 module and RMAAS-2 module which is obtained by combiningthereversible controlled adder/subtractor(RCAS) of different regular manner.

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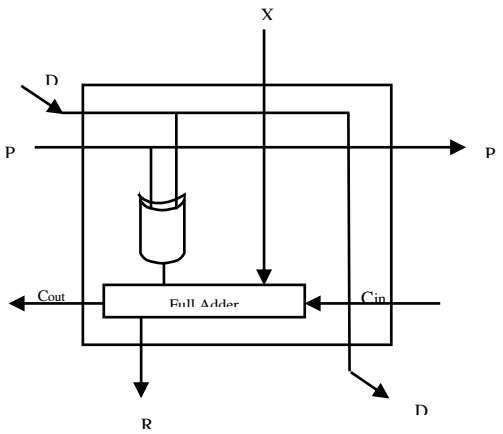

Figure 3 Internal architecture of RCAS block

The fig.3 depicts the internal structure of RCAS block.TheRCAS block is incorporated with One reversible full adder and reversible XOR gate. The addition is performed amonginput X, Cin and output of XOR gate. The full adder's Coutis supplied into the Cinof the next RCAS block.

3.2 RMAAS 1 module

Each RMAAS 1 module madeupof seven RCAS blocks stacked in two rows.Fig 4 depicts the internal structure of RMAAS 1 module.

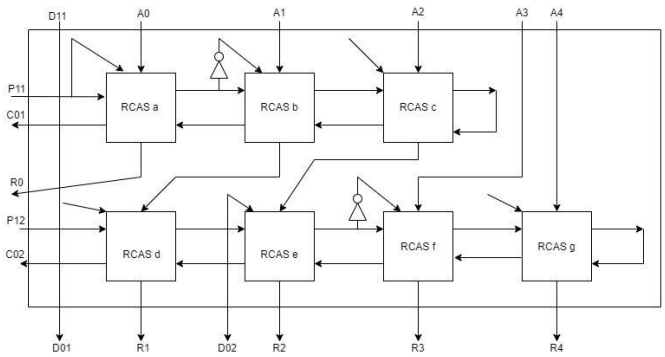

Fig4Internal architecture of RMAAS 1

To do the preliminary subtraction needed by the procedure, set P11 = 1 to the value 1.In addition, by setting A0 = 1, RCAS transfers only the input carry to the output and does not perform any other function. CO1 must be connected to PI2 since the first row's carry out is sent to the second row's P input.The square root is evidenced in the CO1 and CO2 outputs, respectively. This is because the radix is 4-bit data transmitted via A1 to A4.
The block box representation of the RMAAS-1 is depicted in fig 5.

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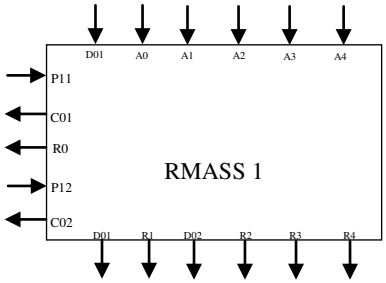


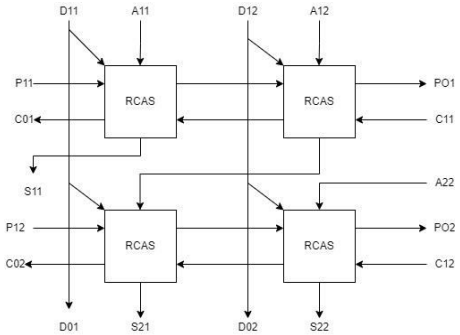
Figure 5 Block diagram of RMAAS 1 module

The input in this case is 0.A1A2A3A4, and the computed square root is Q=0. q1q2, withthe remainder at R1 throughR4.

3.3 RMAAS 2 module

Four RCAS blocks from two consecutive rows make up each RMAAS 2 module.

Fig 6 depicts the internal structure of the RMASS 2 module.Set P11 = 1 to achieve the preliminary subtraction expected by the algorithm.Furthermore, it requires RCAS to merely transmit its input carry to corresponding output and not to perform any other functions.



+Figure 6 Internal architecture of RMAAS 2

CO1 must be connected to P12 in the case where the first row's carry out is sent to the second row's P input.

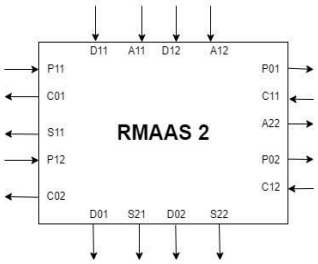


Figure 7Block diagram of RMAAS 2 module

RMAAS 2 module block diagram is illustrated in Figure 7.The output is taken at P12 and C02 now that the input has been given to the module. As a result, a single RMAAS 2 module is definitely capable of performing square root operations.

3.4 Architecture of 8-bit modular non-restoring square rooter

The fig.8 depicts the architecture of 8-bit modular non-restoring square rooter.For the purpose of computing the first bit of the square root, perform 2's complement addition between A1A2 and 01 with the help of q1.

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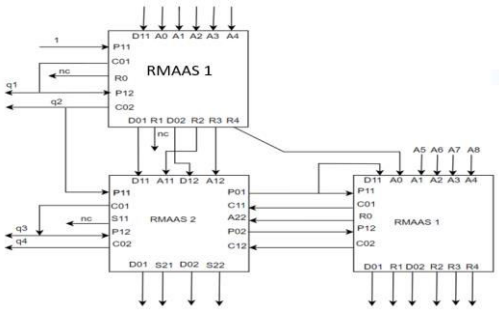

Figure 8 Modular non- restoring square rooter

CO1's carryout is represented by r11r12, but r11r12 is also the 2-bit partial remainder of the initial row, which is represented
by q1 .If q1 is 1, perform (r11r12A3A4 + (0q101)) to obtain the second bit of the square root q2, and if q1 is 0, perform (r11r12A3A4 + 0q111) to generate the second bit of the square root q2. This four-bit addition is done by R1 to R4. Consequently, a single RMAAS 1 module has become able to carry out a 4-bit square root operation, which is a significant improvement.Here, the eight inputs of 8bit modular non-restoring square rooter are A_1,A_2,A_3,A_4,A_5,A_6,A_7 and A_8.Assign the default value 1 to D_{11} and A_0. The result of 8-bit MRNR the square rooter isobtainedin q_1, q_2, q_3 and q_4.

3.5 General architecture of4n-bit modular square rooter

The General architecture of 4n-bit MRNR is demonstrated in Figure 9.

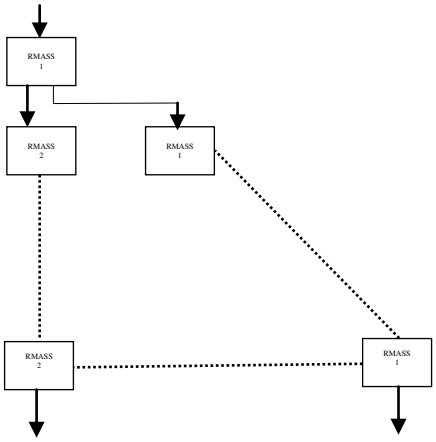

Figure 9 General architecture

In the architecture of square rooter, the left corner of every row should be always RMAAS 1 module and the remaining module should be RMAAS 2 module.By using the above general architecture of square rooter, n-bit square root can be calculated.Where n bit gives the number of rows in the architecture.In order to realize the same, it requires n RMAAS-1 and n(n-1)/2 RMAAS-2 modules respectively.

IV. RESULTS AND DISCUSSION

Modelsim 5.7g has been used to design and simulate the Modular Non-Restoring Square Rooter. Analysis of parameters such as the quantity of reversible gates, the quantum cost, and the garbage outputs were calculated. Device utilization was computed using Quartus-II 9.0 with respect to Stratix-II device along with EP2S15F484C5 family.

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4.1SIMULATION OF PIPELINED 64 BIT KMD GATE4

The simulation result of 64-bit reversible MRNR using KMD gate 4 is represented in Figure 10.
The simulationresult based on the test data is shown below.
For the input,
Input=0000000000000000000000000000000000000000000001111110100000010010 0 $(1036324)_{10}$

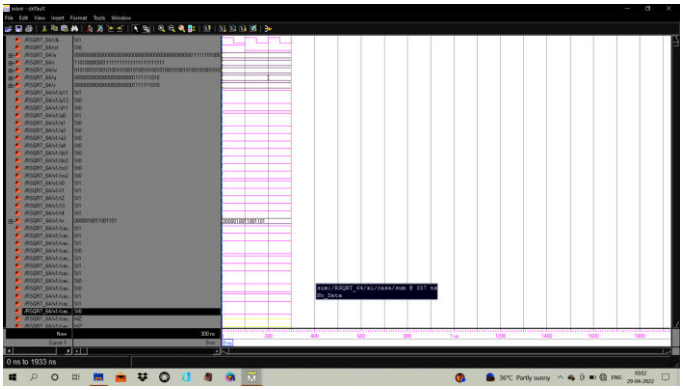

Figure 10 Simulation Result Of 64-Bit KMD Gate 4

The output obtained is
Output =00000000000000000000001111111010$(1018)_{10}$

4.3 SIMULATION OF PIPELINED 64 BIT F2PG GATE

Simulation results for a 64-bit pipelined MRNR using F2PG gate is shown in Figure 11.

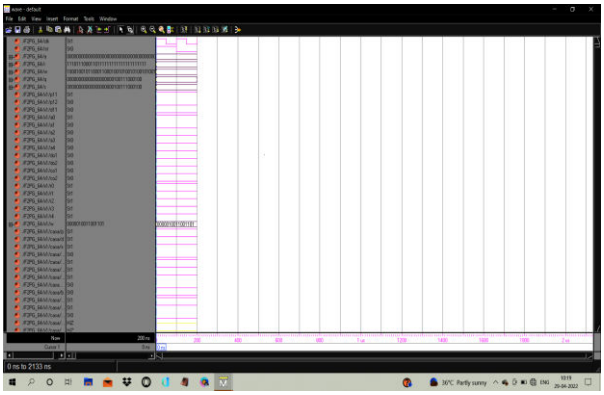

Figure 11 Simulation of 64bit F2PG gate

Evidently, the latency is one clock cycle based on the results.The test data along with simulation result obtained is listed below.
Input=0000000000000000000000000000000000000000000010111
110101111000010000 $(6250000)_{10}$

The output obtained isOutput=0000000000000000000001001110001 00 $(2500)_{10}$

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4.4 SIMULATION OF PIPELINED 64-BITISLAM GATE

The simulation result of a pipelined MRNR using 64-bit Islam gate is depicted in Figure 12.

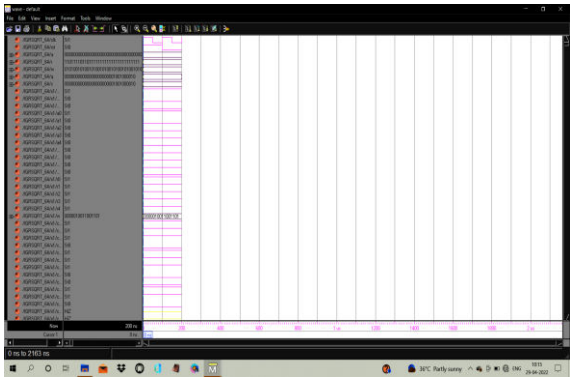

Figure 12simulation of 64bit Islam gate

Below is the test data for the simulationresult.
For the input,
Input= $00000000000000000000000000000000000000000000000010100011010000010 0(167172)_{10}$
The output obtained isOutput = $00000000000000000000001001000010(578)_{10}$

Fault Tolerant Reversible gate	Conventional Non-Restoring Division (CNR)								Modular Non-Restoring Division (MRNR)							
	Number of Reversible gates				Quantum cost				Number of Reversible gates				Quantum cost			
	Word length								Word length							
	8	16	32	64	8	16	32	64	8	16	32	64	8	16	32	64
Islam Gate	60	216	816	3168	420	1512	5712	22176	554	1156	5504	11704	3378	11092	33528	111928
F2PG gate	20	72	272	1056	280	1008	3808	14784	18	52	168	568	252	728	2352	7952
KMD Gate 4	20	72	272	1056	240	864	3264	12672	18	52	168	568	216	624	2016	6816

4.5PERFORMANCE EVALUATION OF FULL ADDER

The comparative study of performance evaluation among the three different gates based on the full adder is presented in Table 1.

Table 1 Performance Of 1-Bit Full Adder

In order to realize a full adder number of KMD gate 4 and F2PG required is 1, whereas to realize the same two Islam gates are required.

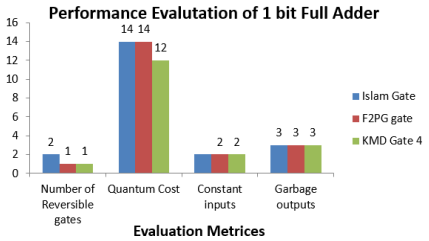

Figure 13 Performance Of 1-Bit Full Adder

The evaluation metrics for a 1-bit full adder are depicted in Fig13. Islam gate, F2RG gate, KMD gate has a quantum cost of 14, 14, 12 respectively. Constant input of Islam gate, F2PG gate and KMD gate4 are two.

4.6 PERFORMANCE EVALUATION OF RCAS BLOCK

The Table 2presents the performance evaluation of RCAS block for Pipelined architecture for KMD gate4, Islam, F2PG.

Fault Tolerant Reversible gate	Number of Reversible gates	Quantum cost
Islam Gate	3	21
F2PG gate	1	14
KMD Gate 4	1	12

Table 2 Performance Of RCAS Block

To design 1 RCAS block using KMD gate4, Islam and F2PG gate, one, three and one reversible gate is required respectively.

Fault Tolerant Reversible gate	Number of Reversible gates	Quantum Cost	Constant inputs	Garbage outputs
Islam Gate	2	14	2	3
F2PG gate	1	14	2	3
KMD gate 4	1	12	2	3

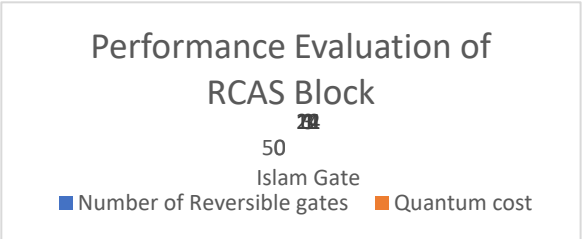

Figure 14 Performance Evaluation OfRCAS Block

Fig.14 depicts the performance metrics of RCAS block. The quantum cost of Islam gate,F2PG gate,KMD gate 4 are 21,14,12 respectively for one RCAS block.

4.7 COMPARISON BETWEEN REVERSIBLE GATES

The Table 3depicts the comparative study of conventional and Modular Non-Restoring square rooter for KMD gate4, Islam, F2PG.

On comparison it can be concluded that amount of reversible gates are reduced in MRNR. To construct an8-bitsquare rooter, it necessitates two RMAAS1 and one RMAAS2. Hence 54 gates are needed in total. The quantum cost of MRNR square rooter for 8 bit using Islam gateis 378 (Number of reversible gates X Quantum gate (54 x 7)). Quantum costs of variable word length can be determined in a similar manner.

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4.8 IMPROVEMENT BETWEEN GATES

The Table 4depicts the comparative evaluation of percentage improvement of KMDgate4, Islam, F2PG.

Parameter	% Of Improvement		
	IG vs F2PGgate	F2PG vs KMD gate 4	KMD gate 4 vs IG
Quantum Cost	33.33	14.29	42.86

with quantum cost as the parameter, it is observed that f2pg gate is 33.33% better than ig gate. similarly, kmd gate 4 is 14.29 % better than f2pg gate and ig gate gives 42.86 % better than performance than kmd gate 4.the graphical representation of percent of the improvement between the gates is depicted in the below fig.15.

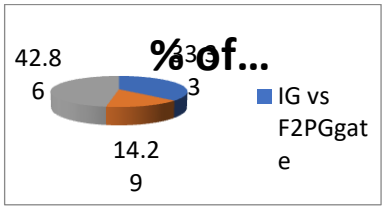

Figure 15 Improvement Between Gates

V. IMPROVEMENT BETWEEN BITS

The Table V depicts the comparative evaluation of percentageimprovement between bits of KMDgate4, F2PG and Islam gate.In the modular non restoring square rooter, the percentage of improvement for 8 bit is 10.Between Reversible GatesFor 16bit, percentage ofimprovement for 8 bit is 10.for 16bit, percentage of improvement is 27.2.

TABLEVPERCENTAGEOF IMPROVEMENT BETWEEN BITS

Parameter	Word length			
	8	16	32	64
Percentage of Improvement	10	27.7	38.25	46.21

The graphical representation of percentage ofthe improvement between bits of the KMDgate4, Islam, F2RG gatesare shown in the following fig.16.

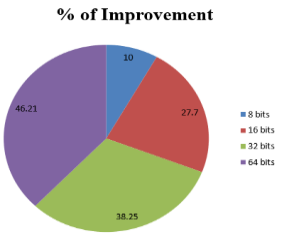

Fig. 16 Improvement between bits

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Improvement is directionally proportional to number of bits.The percentage of improvement for 32 and 64 bits are 38.25,46.21 respectively.

1.COMPARISON BETWEEN CNR AND MRNR

The Table VI shows the comparison between the conventional and the modular non-restoring method based the CAS block utilization.

TABLE VIcomparion between cnr and mrnr**Error! Not a valid link.**The graphical representation of the comparison between the CNR and MRNR is shown in fig.17. By that comparison, the RCAS blocks are reduced considerably in modular non-restoring.

1.LOGIC UTILIZATION

The tabulation forthecomparison among the Gates of ALUT is depicted in Fig 18.

VI. COMPARISION AMOUNG GATES

TABLE

Parameter	Modular Non-Restoring Division (MRNR)			
	ALUT			
	Word length			
	8	16	32	64
Islam gate	10	58	251	1170
F2PG gate	8	56	263	1171
KMD gate4	6	50	222	950

The Fig 18 depicts the ALUT utilization of Islam gate,KMD gate 4 and F2PG gate.

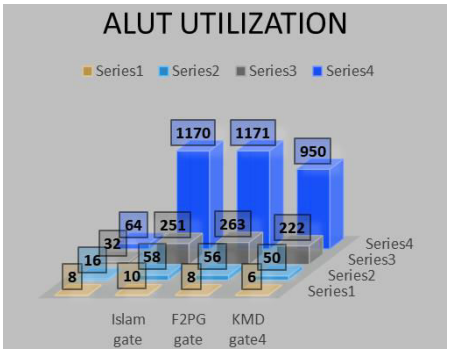

Fig.18 ALUT utilization

The statisticalresults for 64-bit pipelined MRNR states that KMD gate4 utilizes lesser hardware when compared to F2PG gate and Islam gate by 18.80% and 18.87% respectively.

K. TECHNOLOGY MAP VIEWER

Technology Map Viewer demonstrates the internal structure of the design netlist, either after fitting or after Analysis & Synthesis.

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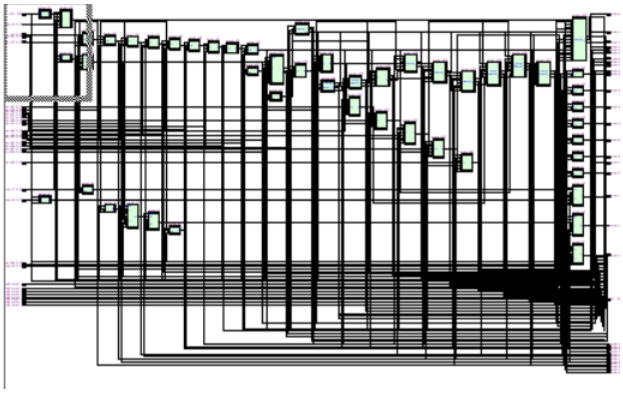

Fig.19 Technology map viewer

The fig.19 represents the technology map viewer of MRNR. Technology Map Viewer depicts the design's hierarchy of device logic cells and I/O ports.

VII. CONCLUSION

The square root is a crucial mathematical operation with numerous applications such as Computer graphics, "GPS" global positioning systems, digital signal processing (DSP) calculations. Proposed modular non restoring square rooter using KMD gate 4 was simulated using Modelsim 5.7g. Device utilization was computed using Quartus-II 9.0 with respect to Stratix-II device along with EP2S15F484C5 as its family.It was found that as the word length increases the efficiency for, the Pipelined Modular Non-Restoring Square rooter (MRNR) among 8, 16, 32 and 64 bits by 10.7%, 27.2%,38.25% and 46.21% respectively. Moreover 64-bit pipelined MRNR using KMD gate4 utilizes lesser hardware when compared to F2PG gate and Islam gate by 18.80% and 18.87% respectively.

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